

implant region and the second implant region are formed.

37. (New) The transistor of claim 34, wherein the first implant region and the second implant region are doped by a same source.

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38. (New) A transistor, comprising:  
an emitter having a periphery;  
a base in contact with the emitter;  
a collector in contact with the base; and  
means for minimizing carrier injection from the periphery of the emitter region to the collector region at high current operation of the transistor.

39. (New) The transistor of claim 38, wherein means for minimizing carrier injection includes an implant region intermediate the base and the collector, the implant region having an implant surface area greater than a surface area of the emitter and less than a surface area of the base.

40. (New) A transistor, comprising:  
an emitter;  
a base in contact with the emitter;  
a collector in contact with the base; and  
means for minimizing base-collector capacitance and maximizing high current operation.

41. (New) The transistor of claim 40, wherein means for minimizing base-collector capacitance and maximizing high current operation includes an implant region intermediate the base and the collector, the implant region having an implant surface area greater than a surface area of the emitter and less than a surface area of the base.